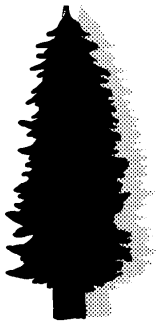


SCIPP 99/55
December 23, 1999

User Guide for the GLAST Beam Test Tracker

W. Kröger and M. Hirayama
Santa Cruz Institute for Particle Physics
University of California, Santa Cruz

Abstract

The GLAST beam test silicon tracker was built to confirm performance of the tracker and feasibility of the tracker fabrication and operation. The tracker will be intensively tested at SLAC using a test beam. This document describes hardware components of the tracker, beam test setup, tracker operation, and readout scheme. Detailed information of the tracker operations is also provided in later sections.

1 How to Read This User Guide

This document consists of three parts. First, a tracker part of the beam test setup is shown in section 2. Then, sections 3 and 4 briefly describes tracker hardware components, tracker operation, and readout scheme. These sections are of interest for everyone that has to interact with the tracker. And finally, section 5 describes more detailed information of tracker operation. The section can be a reference for tracker experts.

It is not necessary for everyone to read through all of this document. The part of the document you should read depends on what extent you are operating the tracker to. From that point of view, there are three different types of users that will operate the tracker. 1) Shift takers. These people are responsible to ensure that the tracker is running properly during data taking. Those users are recommended to read section 2 Sections 3 and 4 can be interesting for better understanding of the tracker. 2) Tracker users. These people are calibrating and understanding the tracker. They monitor the data and modify the tracker configuration, such as masking channels and setting threshold voltages, depending on the tracker status. The tracker users are required to understand all the subjects covered by this document. 3) Tracker developers. These people take a lead in setting up the tracker, changing the setup, planning and revising a run plan. Section 5 will be references for the tracker developers.

2 Beam Test Setup

In the beam test, the tracker is controlled by a TKR TEM board in a VME crate called TKR VME (Figure 1). Eight shielded cables connect the TEM board to tracker readout electronics through eight repeater boards. The repeater board is a small printed-circuit board attached to the base plate of the tracker, to buffer signals from the tracker and to filter the power supply lines (See section 3 for more explanations). All the electrical connection for the tracker, such as power lines and signal lines, are on those eight cables.

Detector bias and power for readout electronics are supplied by two power supplies connected to the TEM board. The detector bias is provided by one high voltage supply Keithley 2400. An HP 6629A DC power supply is used for the front-end electronic power: DVDD (digital power), AVDD (analog power), and AVDD2 (2nd analog power). The repeater boards are powered from the digital power DVDD. The TKR VME crate also includes a CPU board with an Ethernet port. On the CPU board, VxWorks is running as an operating system to control and access the TKR TEM board. The VxWorks system is controlled through the Ethernet connection.

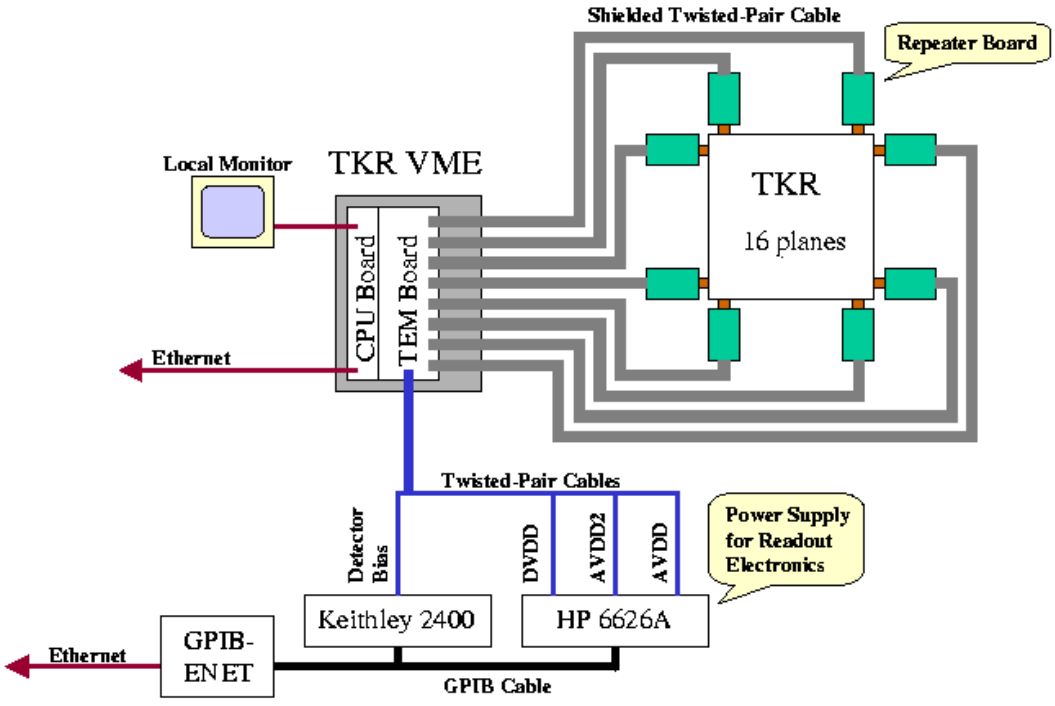


Fig. 1. Schematic drawing of beam test setup for tracker

To power on the tracker, the HP 6629A should be powered on first, the VME crate second, and Keithley 2400 the last. For detector bias, check compliance level before output the voltage, start with relatively low voltage like 2 V, slowly raise the voltage with watching detector current every time you raise the voltage. To be safe, raise the bias with 1 V step up to 10 V and with 10 V step afterwards. You might see detector current reach compliance level when you raise the voltage. You should wait for a couple of seconds until detector current gets down below compliance level before raising it to the next voltage level.

To power off the tracker, the detector voltage should be lowered slowly, say, with 10 V step a second or so. After turning off the bias voltage, turn off the VME crate, then HP 6629A.

Here is a list of instruments for the tracker part of the setup below. Also, setting of power supplies are shown in Table 1 with typical currents listed.

Tracker Described in section 3.

TKR VME The VME crate including a TKR TEM board and a CPU board with an Ethernet access to control the TEM board. A local monitor will be attached for booting the system.

Power Supply for readout electronics An HP 6624A power supply is used for front-end electronic power. Three channels are needed for the digital power (DVDD), the analog power (AVDD), and the 2nd analog power (AVDD2). The repeater board is powered from the digital power (DVDD).

Power Supply for Detector Bias One Keithley 2400 supplies detector bias to all the detectors.

GPIB-ENET An Ethernet-to-GPIB controller by National Instruments to control the power supplies from Ethernet.

Table 1. Power Supplies for the Beam Test Setup

		Voltage @		
Power Supply	Power	Supply	Repeater board [a)]	Typical Current
HP 6629A	DVDD	+3.3 V	$\approx$ 3.0 V	1.4 A
	AVDD2	+2.2 V	$\approx$ 2.0 V	1.2 A
	AVDD	+5.2 V	$\approx$ 5.0 V	0.8–0.9 A
Keithley 2400	Detector Bias	+100 V	—	100–170 μA

a) The voltages drop by 100–300 mV along the cables due to currents of $\approx$ 1 A on DVDD, AVDD, and AVDD2.

3 Beam Test Tracker

In this section, the tracker hardware configuration is described. The beam test tracker consists of 17 detector trays stacked on top of each other. On each tray silicon strip detectors, lead sheets for pair conversion, and readout electronics are mounted. The trays are electrically interconnected with 8 Kapton cables attached on 4 sides of the tracker, which connects all the electronics to a tower controller. Below in this section, each component is described in more detail.

3.1 Detector Layer

Silicon strip detectors are mounted on the top and the bottom side of a detector tray. A set of detectors on one side of a tray forms a detector layer measuring X or Y of a track. An x-y plane is formed between two trays when one is stacked on the other; a top layer of the lower tray and a bottom layer of the upper tray forms an x-y plane. Of the 17 trays, the top-most tray carries detectors only on its bottom side, and the bottom-most tray only on its top side. Detectors are mounted on the both side on the rest of fifteen trays. In the beam test tracker there are 32 layers which form 16 x-y planes, in total.

A silicon detector layer consists of 3, 4, or 5 detector ladders depending on the location of the layer, where a detector ladder consists either of five 4-inch detectors or of three 6-inch detectors glued and wire-bonded together. A 4-inch detector is a square strip detector of 6.4 cm by 6.4 cm with 320 p^+ strips at 195 μm pitch, and a 6-inch one is rectangle, 6.4 cm wide and 10.68 cm long, with the same number of strips with the same pitch as a 4-inch detector. This was designed so that both of five 4-inch detectors and three 6-inch detectors form a detector ladder 6.4 cm wide and 32 cm long. And five detector ladders will cover a square region of 32 cm by 32 cm with 1600 strips. In the tracker 130 ladders are used in total; 50 ladders of them are of 4-inch detectors (250 detectors) and 80 of 6-inch detectors (240 detectors).

Of the 16 x-y planes 8 planes from the top of the tracker are only partially covered by detectors; the top 7 planes consist of three ladders on each of X- and Y-measuring layer (3×3 plane) and the 8th plane from the top of the tracker consists of four ladders on each (4×4 plane). The rest of 8 planes are fully covered, namely, five ladders are on both layers (5×5 plane).

Also, on the upstream side of each x-y plane there is a lead converter. There are three different thicknesses, 3.5 % radiation length (normal thickness), 25 % radiation length (called "super GLAST"), and 0 % radiation length (or no lead sheet). The 3.5 % lead sheets are placed on the top 11 planes and the 25 % lead sheets are on the 12th, 13th, and 14th planes. There is no lead sheet placed in front of the bottom two planes.

3.2 Tray Stack and Tracker Coordinate

The 17 trays are stacked up with every 2nd tray rotated by 90 degree to form an x-y plane between trays. The bottom-most tray is bolted to a base plate of the tracker and the orientation of the bottom-most tray in reference to the base plate is unique. The 2nd tray from the bottom is rotated by 90 degree clockwise in reference to the bottom-most tray. The 3rd tray is stacked in the same orientation as the bottom-most tray, the 4th tray is in the same orientation as the 2nd tray, and so on. This gives you the top-most tray being placed in the same orientation as the bottom-most tray.

On each tray X or Y of a track is measured. A layer on the bottom-most tray is measuring Y. Both layers on the 2nd tray from the bottom then measure X. Layers on the 3rd tray measure Y, ones on the 4th X, and so on. This gives you a layer on the top-most tray measuring Y. The X- or Y-coordinate increases from the left side towards the right side on a tray, where a left side of the tray is defined as the left side when you look at the top side of the tray with a readout electronics for a top side layer set at the bottom of your view. The left-most strip always has a strip number 0 on both sides of a tray, no matter which axis it measures. A strip number ranges from 0 to 1599 on a full tray, from 0 to 1279 on a 4×4 tray, and from 0 to 959 on a 3×3 tray.

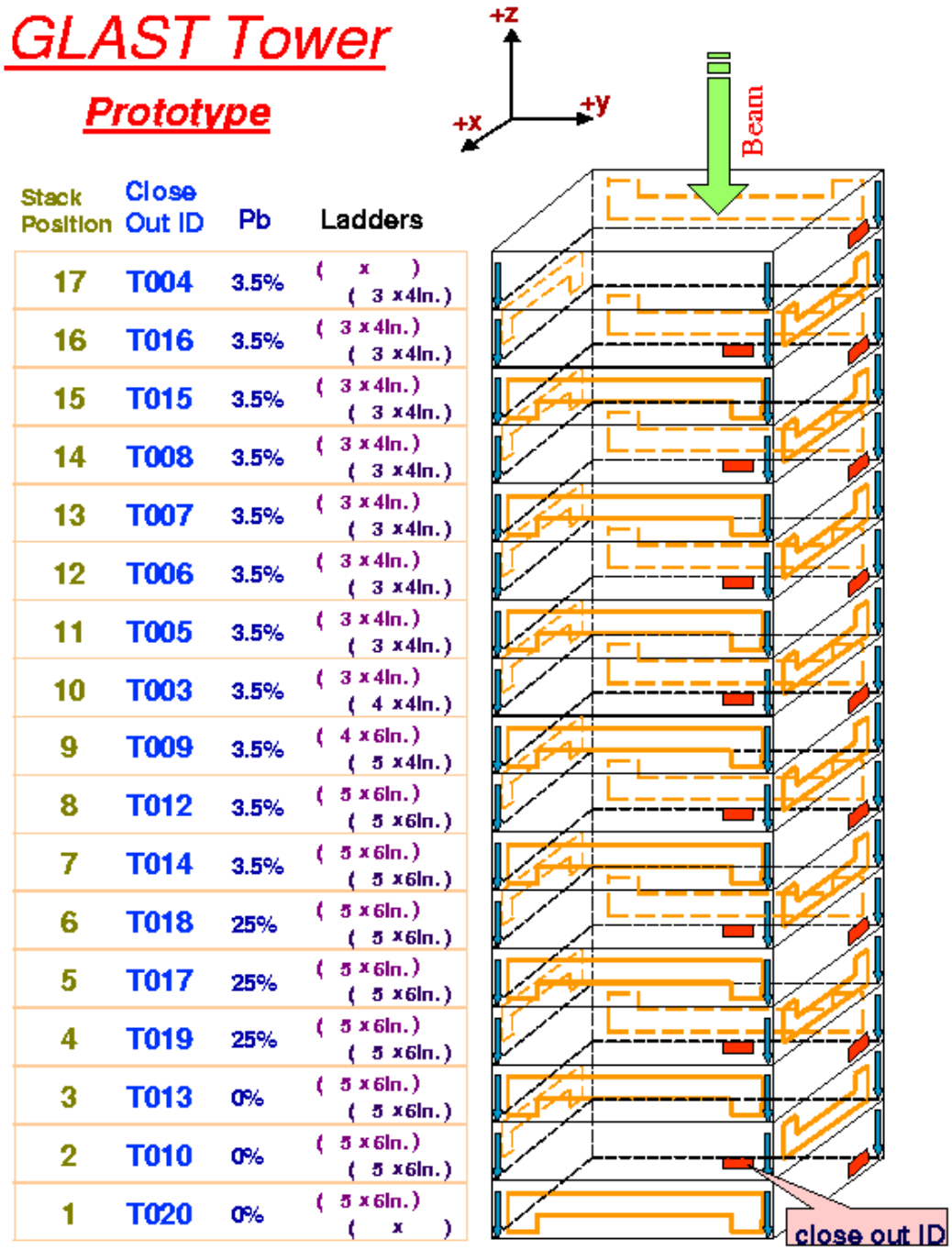
The Z-axis of the tracker is defined as an axis going from the bottom to the top of the tracker. In the beam test the beam is incident from the top of the tracker with normal incident configuration, namely, the beam travels $-$Z direction. The plane number is assigned to each x-y plane starting with 0 increasing in +Z direction. Therefore, the beam hits Plane 15 first and Plane 0 last.

Table 2 summarizes the detector configuration of the tracker. Figure 2 shows the tray stack and the tracker coordinate system. Also, figures 3-6 shows detector coverage of each x-y plane with ID numbers of tray components indicated.

3.3 Readout Electronics

Each silicon layer is read out by a high density interface (HDI), which is a printed circuit board with 25 front-end chips (GTFE64), two controller chips (GTRC), and passive components mounted. Two HDI's are attached on two sides of a tray, one on a side to read out a layer on the top side of the tray and the other on the opposite side to read out one on the bottom. The top-most and the bottom-most tray has only one HDI attached, since detectors are mounted only on one side of the tray. There are 32 HDI's in total with 64 controller chips and 800 front-end chips.

Each front-end chip reads out 64 strips, which covers 1600 strips with 25 chips on an HDI. Hit information of the 1600 strips is recorded for every trigger and kept in 8-deep data buffers of the front-end chips until it is read out. The data



Stack Position	Close Out ID	Pb	Ladders
17	T004	3.5%	(x) (3 x4In.)
16	T016	3.5%	(3 x4In.) (3 x4In.)
15	T015	3.5%	(3 x4In.) (3 x4In.)
14	T008	3.5%	(3 x4In.) (3 x4In.)
13	T007	3.5%	(3 x4In.) (3 x4In.)
12	T006	3.5%	(3 x4In.) (3 x4In.)
11	T005	3.5%	(3 x4In.) (3 x4In.)
10	T003	3.5%	(3 x4In.) (4 x4In.)
9	T009	3.5%	(4 x6In.) (5 x4In.)
8	T012	3.5%	(5 x6In.) (5 x6In.)
7	T014	3.5%	(5 x6In.) (5 x6In.)
6	T018	25%	(5 x6In.) (5 x6In.)
5	T017	25%	(5 x6In.) (5 x6In.)
4	T019	25%	(5 x6In.) (5 x6In.)
3	T013	0%	(5 x6In.) (5 x6In.)
2	T010	0%	(5 x6In.) (5 x6In.)
1	T020	0%	(5 x6In.) (x)

Fig. 2. Schematic drawing of the tray stack.

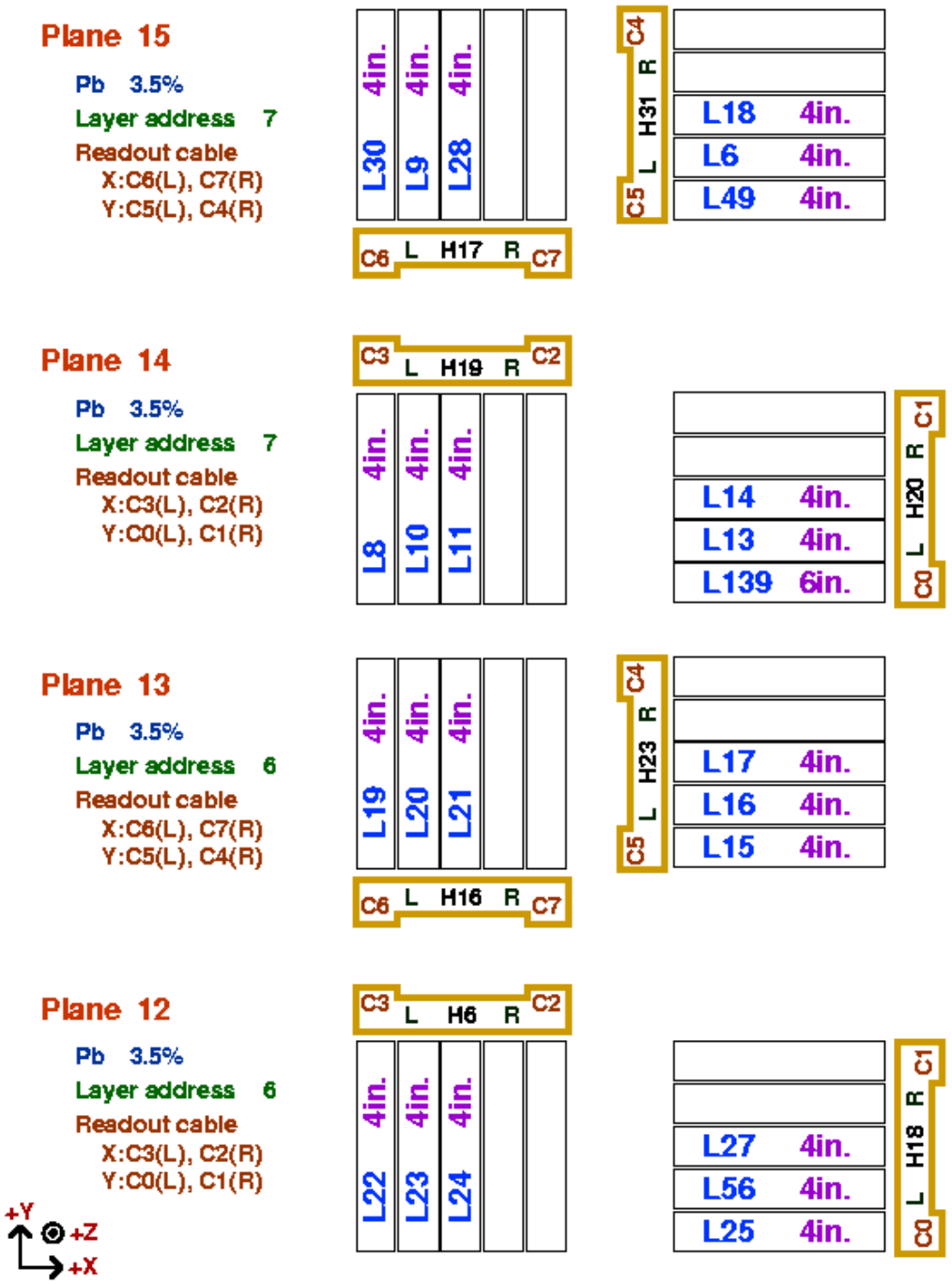


Fig. 3. Schematic drawing of x-y planes. On each plane, detector coverage of X- and Y-layers are shown. Also, a readout electronics (HDI) is drawn next to each layer to show which side of the layer the readout electronics attached. In the figure, detector ladder ID's, HDI ID's, and Kapton cable ID's are also shown.

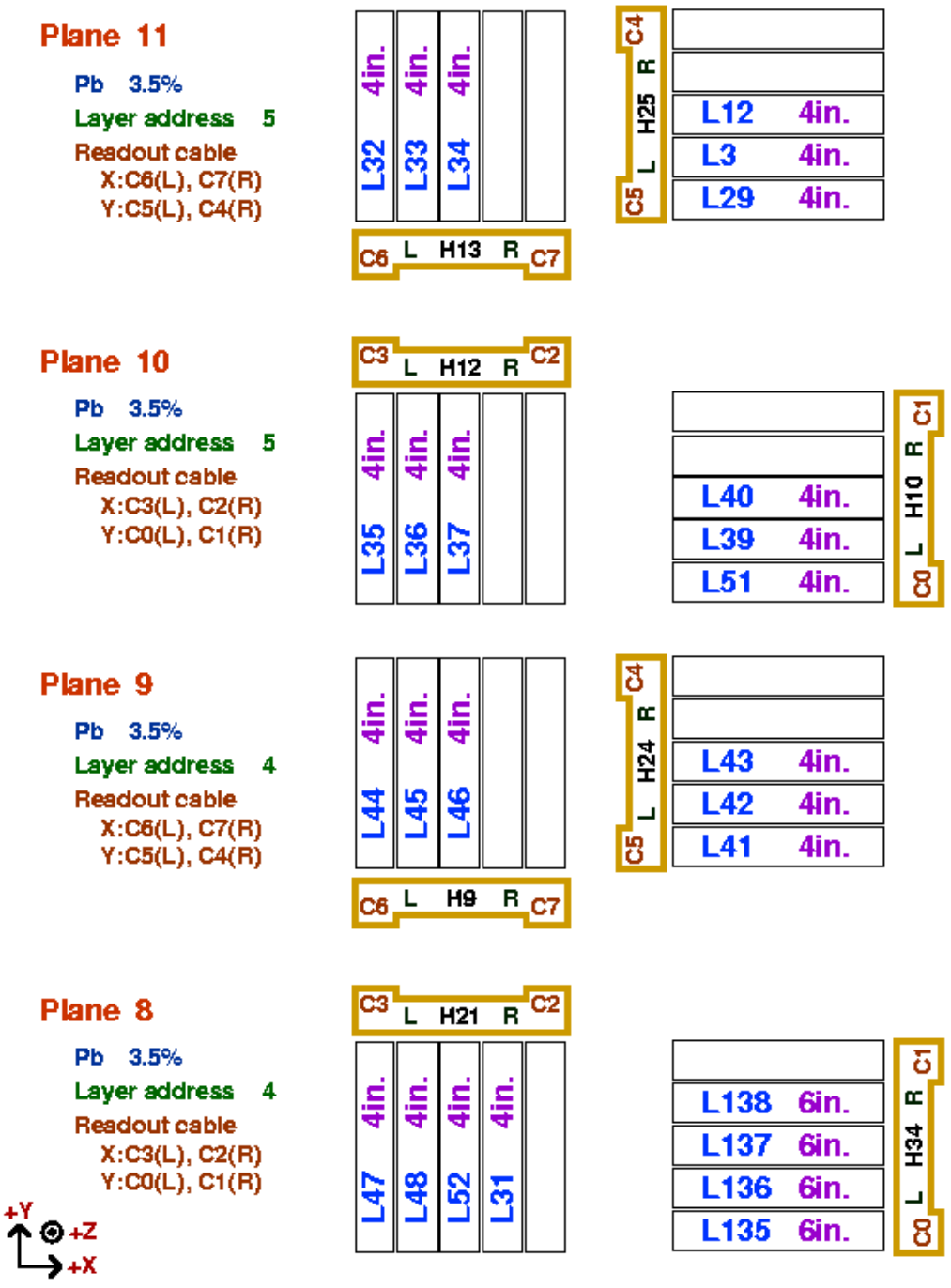


Fig. 4. Schematic drawing of x-y planes (cont.)

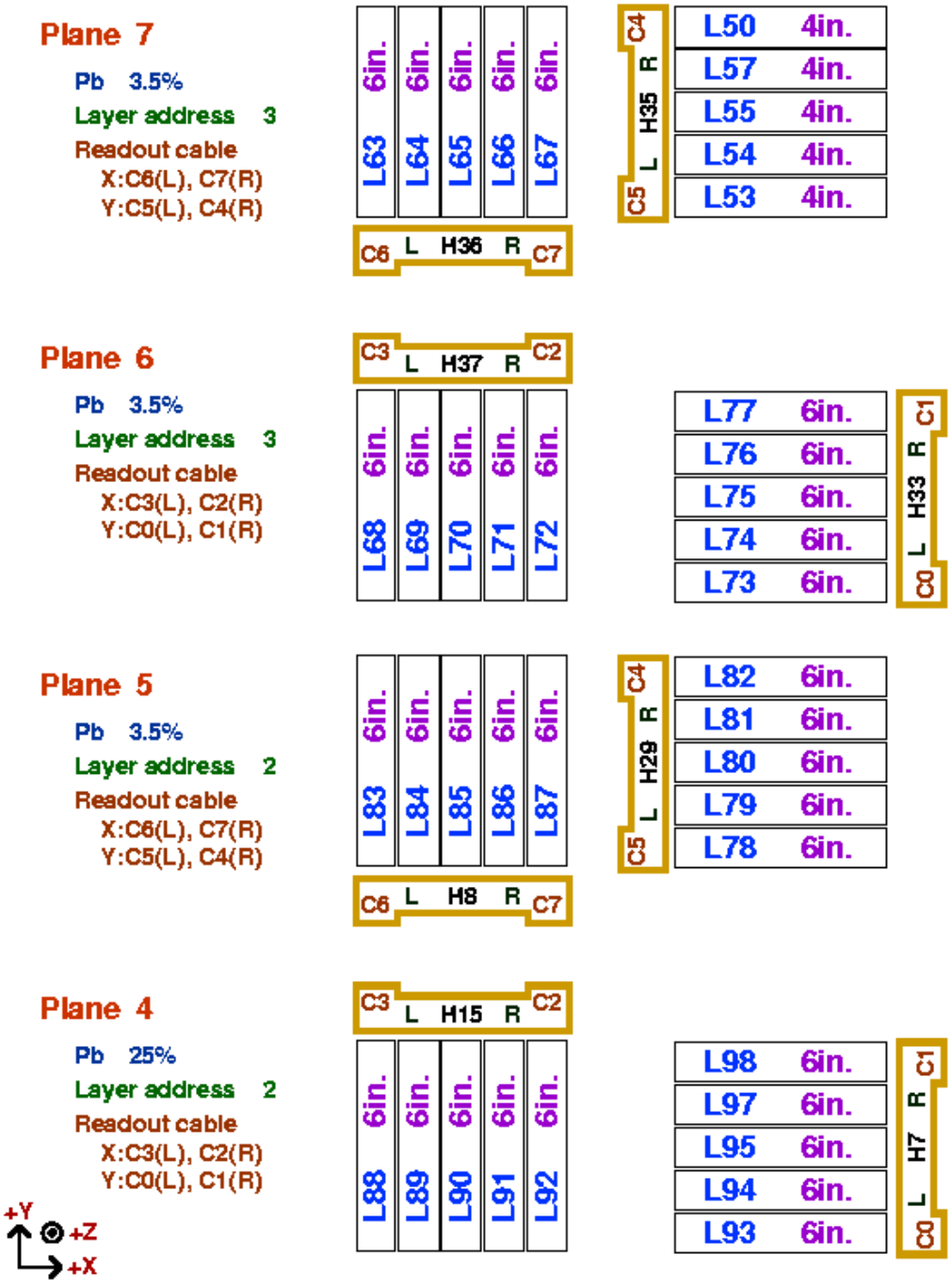


Fig. 5. Schematic drawing of x-y planes (cont.)

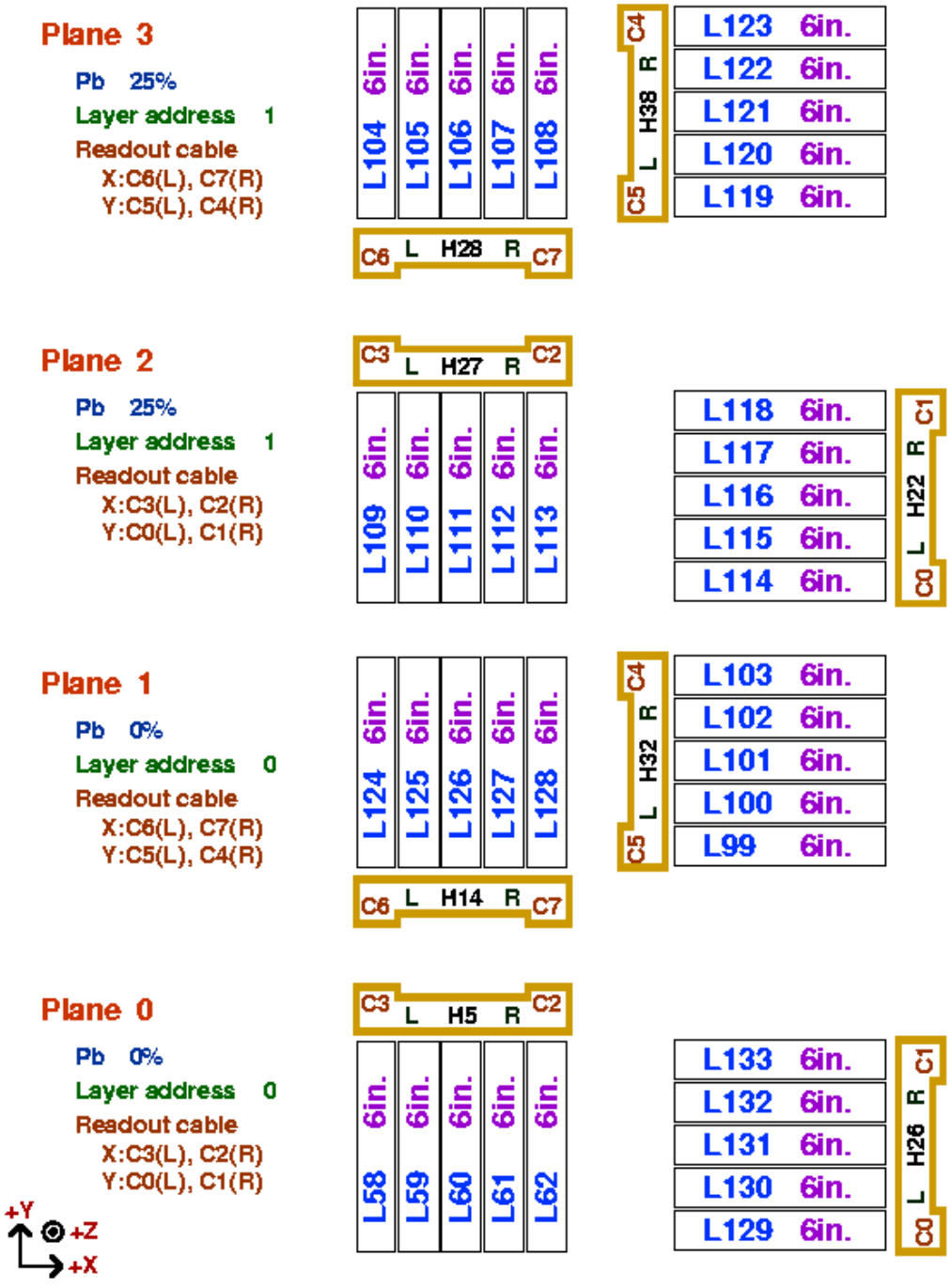


Fig. 6. Schematic drawing of x-y planes (cont.)

Table 2. Summary of 16 x-y planes of the tracker

		Active strip # in layer [a)]	
	Pb thickness	Top layer	Bottom layer
Plane 15	3.5 % R.L.	0-959 (Y)	0-959 (X)
Plane 14	3.5 % R.L.	0-959 (X)	0-959 (Y)
Plane 13	3.5 % R.L.	0-959 (Y)	0-959 (X)
Plane 12	3.5 % R.L.	0-959 (X)	0-959 (Y)
Plane 11	3.5 % R.L.	0-959 (Y)	0-959 (X)
Plane 10	3.5 % R.L.	0-959 (X)	0-959 (Y)
Plane 9	3.5 % R.L.	0-959 (Y)	0-959 (X)
Plane 8	3.5 % R.L.	0-1279 (X)	0-1279 (Y)
Plane 7	3.5 % R.L.	0-1599 (Y)	0-1599 (X)
Plane 6	3.5 % R.L.	0-1599 (X)	0-1599 (Y)
Plane 5	3.5 % R.L.	0-1599 (Y)	0-1599 (X)
Plane 4	25 % R.L.	0-1599 (X)	0-1599 (Y)
Plane 3	25 % R.L.	0-1599 (Y)	0-1599 (X)
Plane 2	25 % R.L.	0-1599 (X)	0-1599 (Y)
Plane 1	0 % R.L.	0-1599 (Y)	0-1599 (X)
Plane 0	0 % R.L.	0-1599 (X)	0-1599 (Y)

a) Measuring axis in parentheses

is read out by one of the controller chips. During readout, a front-end chip sends out the data to a neighboring chip, either on the right or on the left, and the neighbor passes it to the next neighbor. Readout direction can be set by command to individual front-end chip. The hit data is transfered in this manner all the way through the HDI until the last chip passes it to one of the controller chips.

Two controller chips on an HDI control all front-end chips on the HDI. One chip locates on the left side of an HDI and reads out left-going data, while the other on the right and reads out right-going data. Both of the controller chips can read out either the entire side of the tray or a part of it. Arbitrary number of front-end chips can be assigned to be read out from the left side or the right side of an HDI.

A controller chip is also an interface to a tower electronics module (TEM). It receives commands from a TEM board and sends out hit information to a TEM board after it reads out front-end chips and converts data format. These communication are made through a Kapton flexible cable connecting HDI's to a TEM board through a repeater board which buffers weak signals from HDI's. There are 8 HDI's on each of four sides of the tracker. A set of 8 HDI's is daisy-chained and

connected to a TEM board with a Kapton cable. The left side controller chip and the right side one are connected independently, there are 8 cables connected to the TEM board in total.

4 Tracker Operation

The tracker is operated through a TEM board on a VME crate called TKR VME. The tracker can be configured, operated, and readout with the TKR VME system through Ethernet. In response to an event trigger or upon our request sent through Ethernet, the TEM board sends out commands to controller chips on HDI's and reads their responses. The responses include hit information during normal operation. The TEM board interprets the hit information, reformat them, and put them into an event FIFO, which is visible in a VME memory space.

In sections below, tracker readout procedure is briefly explained. Also, a control register of a front-end chip, that of a controller chip, and addressing scheme for both chips are described.

4.1 Readout Procedure

To operate the tracker, all the HDI's must be configured at first. All control parameters, such as threshold, must be set by writing them into a control register of a front-end chip or that of a controller chip. Contents of control registers are described in a later section.

Once it is configured, the tracker is ready to trigger a DAQ system in response to a particle passing through the tracker. If the amount of charges collected by a strip exceeds threshold, a corresponding channel of a front-end chip issues a fast-OR signal, which is immediately sent to a TEM board. At the same time, the length of the fast-OR signal, called Time-over-Threshold (ToT), is measured by a controller chip in charge of the front-end chip.

The TEM board judges whether to read it out or not. If the TEM board sees a hit (or more) on three consecutive x-y planes, the event should be read out ("3-in-a-row" condition). If and only if the TEM board receives trigger signals from three neighboring planes, it requests a level 1 trigger (L1T) to the DAQ system by sending an L1T request signal. In response to an L1T request, the DAQ system sends out an L1T signal to the TKR TEM board and other TEM boards for other instruments. The TKR TEM board fans out the L1T signal to all the layers in the tracker (trigger acknowledge signal), with which all the front-end chips latch hit status of all the 64 channels and store it to an event FIFO.

The TEM board starts a readout sequence. The TEM board sends a Read-Event command to all the controller chips on the tracker. In response to the command, controller chips automatically issue a Read-Event command to all the front-end chips on their HDI. The front-end chips responds it by extracting the hit status from an event FIFO and shifting it out all the way across the HDI until it gets to a controller chip. A controller chip counts a strip number while it is receiving hit status from front-end chips, and store the strip number into an event

buffer when it is a hit on the channel. A controller chip also stores the time-over-threshold, the number of hits, a frame check sequence, etc., in the event buffer. To discard an event, the TEM board sends a Clear-Event command to all the controller chips, which issues a Clear-Event command to all the front-end chips. The front-end chips will erase the event in FIFO.

For an event to be read out, a TEM board issues a readout token, which is a digital signal given to a controller chip on the lowest layer on a cable. When a controller chip receives a token, it sends out contents of an event buffer to a controller chip on a lower neighboring layer, or to a TEM board in case of the lowest layer, and passes a token to a higher neighboring layer. Through this daisy chain of token/data passing, a TEM board eventually receives all the event buffer contents of eight controller chips on a readout cable one after another, as a readout token is being passed from the bottom controller chip to the top one. Readout procedures on all the eight readout cables takes place simultaneously. A TEM board put them altogether into an event buffer on the board, which can be read out through Ethernet.

Readout sequence for an event can be started anytime after the event, even after another event occurs. However, there is a limitation on the number of events which the tracker can hold until they are readout. A front-end chip can hold eight events and a controller chip has two event buffer. Once the number of events exceed those limits, the oldest event will be lost and overwritten by the new event. It is a TEM board's responsibility to keep track the number of events in front-end chips and in controller chips.

4.2 Tracker Configuration

A front-end chip and a controller chip have its own control register in it to store configuration of a tracker. Contents of control registers of a front-end chip can be re-written by a TEM board at anytime by sending a set-register command to the HDI's.

A front-end chip holds following information in the control register of 207 bits in total. To set a set of parameters to a front-end chip, a TEM board should send a Load-GTFE-Register command to a controller chip on the same HDI as the front-end chip, and let it send a Load-Register command to the front-end chip. Since each front-end chip is addressed uniquely in a tracker, you can write different setting to individual front-end chip.

Calibration mask (64 bits)

Defines channel(s) into which a calibration strobe should be issued. If a channel is masked, no calibration charges will be injected on the channel. Each bit corresponds to a single input channel of the front-end chip.

Channel mask (64 bits)

Defines channel(s) on which a signal from a detector strip should be latched. If a channel is masked, no hit is recorded on the channel. Each bit corresponds to a single input channel of the front-end chip.

Trigger mask (64 bits)

Defines channel(s) which should contribute to a fast-OR signal of the chip. If a channel is masked, no signal on the channel generates a fast-OR signal. Each bit corresponds to a single input channel of the front-end chip.

Calibration DAC setting (7 bits)

Defines the amount of charges injected by a calibration strobe in combination of 6 bit DAC value and 1 bit range selection. Only one value can be set for a chip. Low range and high range are available for threshold DAC. Threshold voltage ranges from 0.3 fC to 19 fC (0.3 fC step) in low range and from 1.2 fC to 77 fC (1.2 fC step) in high range.

Threshold DAC setting (7 bits)

Defines threshold voltage in combination of 6 bit DAC value and 1 bit range selection. Only one threshold voltage can be set for a chip. Low range and high range are available for threshold DAC. Threshold voltage ranges from 6 mV to 380 mV (6 mV step) in low range and from 24 mV to 1.5 V (24 mV step) in high range.

Readout direction (1 bit)

Defines in which direction (left or right) the front-end chip should send out hit information.

A controller chip keeps following information in its control register of 8 bits in total. To set a set of parameters to the controller chip, a TEM board should send a Load-Register command to a controller chip. Since each controller chip is addressed uniquely in a tracker, you can write different setting to individual controller chip.

Readout mode (1 bit)

Defines whether the controller chip should initiate a readout sequence even without a fast-OR signal generated by the layer.

FCS attachment (1 bit)

Defines whether the controller chip should calculate an FCS (Frame Check Sequence) and attach it to data. An FCS is a bit pattern of 11 bits calculated from bit sequence of data being sent with a CRC algorithm. With FCS a receiver of the data can check whether the data is corrupted during transmission.

Number of chips (5 bit)

Defines the number of chips to be read by the controller chip.

Note that settings of readout direction of all the 25 front-end chips and two controller chips on an HDI must be consistent with each other. For example, suppose that you decide to readout the left 12 front-end chips from the left side of one HDI and the rest from the right. Then, you should set control direction of the left 12 front-end chips to "left", that of the rest to "right", and furthermore, you should set the number of chips of the left controller chip to "12" and that of the right one to "13". If you set them otherwise, readout of the HDI may be screwed up.

4.3 Addressing Scheme

In each command sent to a controller chip, there is an address of a controller chip to communicate embedded. The address is called a controller chip address or a layer address. Some commands can be sent to a front-end chip through a controller chip. To do it, a TEM board sends a command to a controller chip to let it send a command to a front-end chip. In such a command, an address of the front-end chip must be included as well as a controller chip address. It is called a front-end address. And each of eight readout cables of the tracker is numbered from C0 to C7, each of which is connected a port 0 to 7 on a front panel of a TEM board.

A combination of three addresses specifies a single front-end chip in a tower: a front-end chip address, a layer address of the layer where the front-end chip belongs to, and a Kapton cable number of the cable which the layer connects to. A front-end chip address ranges 0 through 24 and is unique on an HDI; the left-most front-end chip on an HDI is addressed 0, the 2nd left-most chip 1, ..., the right-most chip 24. A layer address, which is an address of controller chips on the layer, ranges from 0 to 7 and is unique on a Kapton cable; the bottom-most layer on a Kapton cable is addressed 0, ..., the top one 7. Finally, A Kapton cable number ranges 0 through 7 and is unique on the tracker. The cable connecting left sides of HDI's attached on +X side of the tracker is called C0, the one connecting right side of the HDI's C1, and so on (See also Figures 7 and 8 for others).

For a front-end chip address and a layer address, there is a broadcast address, which is 31 as a decimal number. For example, A controller chip accepts a command when an address in the command matches its own address or it is 31. The broadcast address is used to send a command to all the chips on the command bus.

Note that A front-end chip does not accepts a command from the right side controller chip when it is configured to be read out from the left side, and vise versa. This is true even for a command with a broadcast address. So, you should know readout direction of a front-end chip of interest, before you send a command

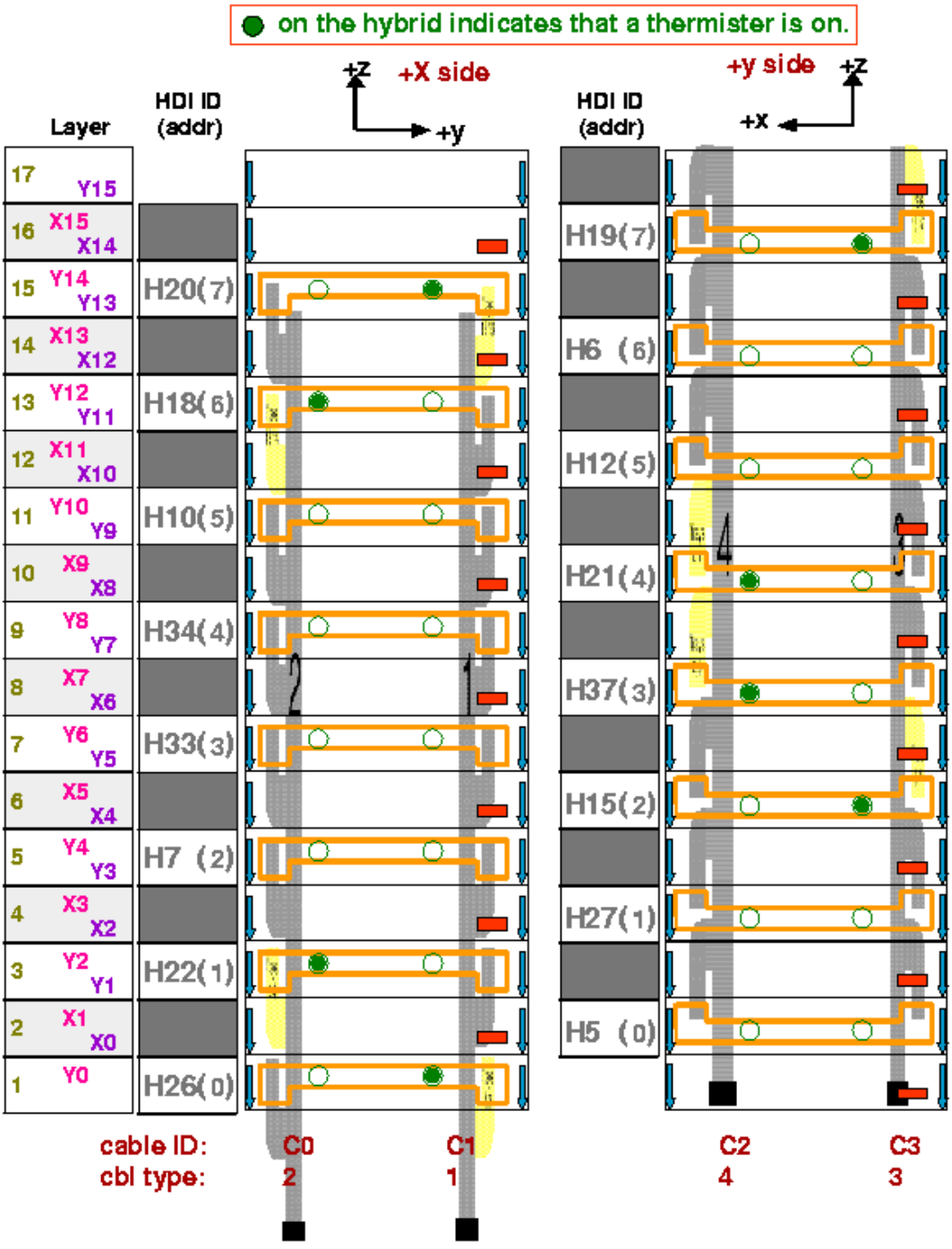


Fig. 7. Schematic drawing of (+X,+Y) side of the tracker

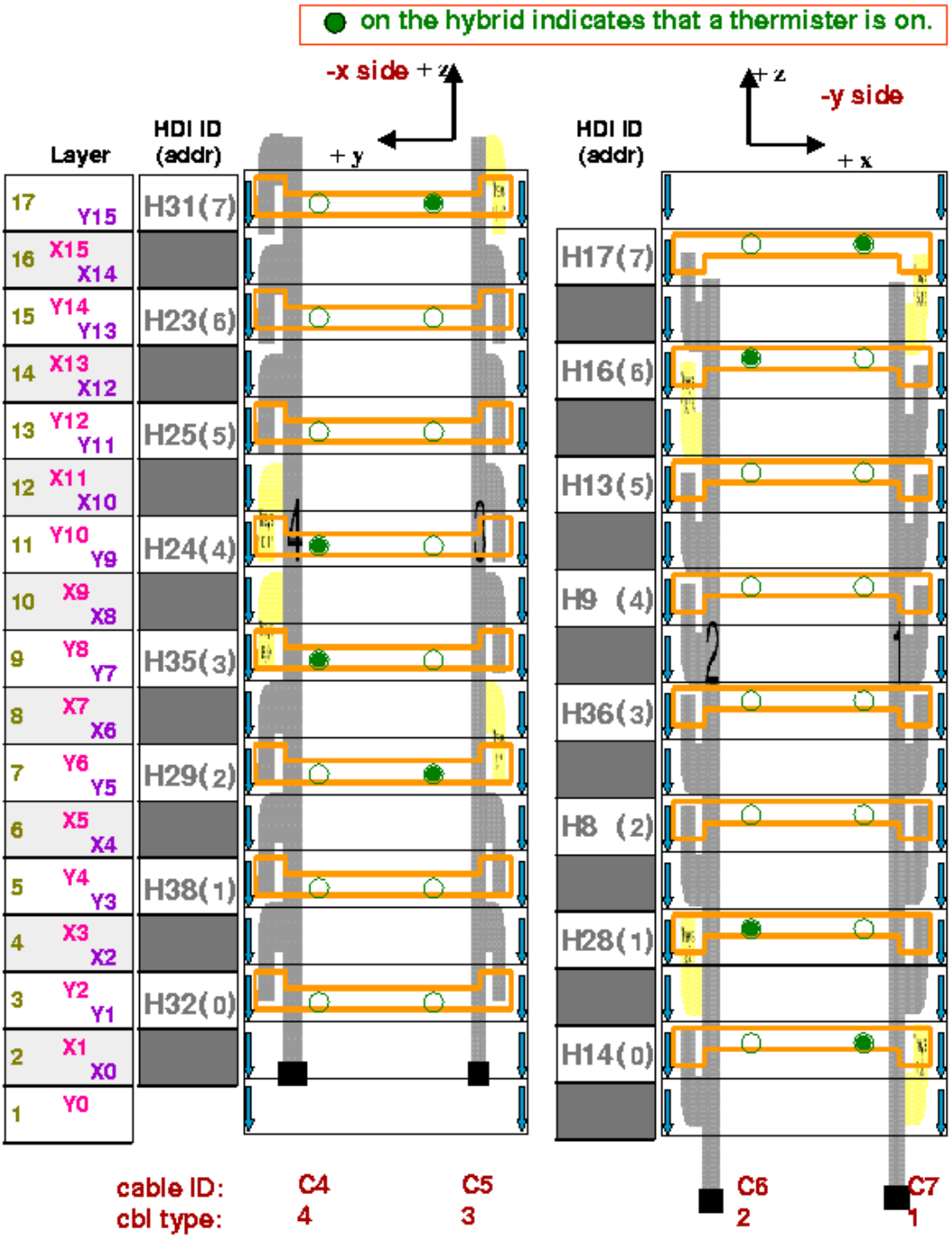


Fig. 8. Schematic drawing of (−X,−Y) side of the tracker

to it, and choose an appropriate controller chip to send a command to. Only one exception on the readout-direction rule is a Load-Register command; it is accepted by a front-end chip no matter which readout direction is set to the front-end chip and no matter which controller chip sends the command to it.

Special consideration should be made when a Load-GTFE-Register command is sent with a broadcast address. If a Load-GTFE-Register command is sent to a controller chip with a specific layer address and a broadcast front-end chip address, a control register of all the front-end chips on the specified layer will be overwritten. If a broadcast address is used both for a controller chip address and for a front-end chip address, all the front-end chips in the tracker will be re-written in one command.

5 Details on Tracker

It is not necessary for shift taker to read this section, if you are not interested in. In this section, details on the tracker is described. This section is a reference for tracker experts.

5.1 Control Register

A control register of a front-end chip consists of 207 bits, which are summarized in Table 3. When a control register is loaded with non-broadcast address, a front-end chip specified with the address outputs previous contents of the register on a CTRLREG output pad (single-ended CMOS signal), with bit 0 first in time. If it is loaded with a broadcast address, no signal is seen on the pad. The bit stream is received by a controller chip and forwarded to data output (DOUT). So far, a TEM board cannot capture nor store this bit stream. So a TEM board should keep track of control register contents of all the front-end chip in the tracker.

During loading a register, an HDI becomes very noisy. Especially, a fast-OR trigger bounces around, namely, many fake trigger signals will be seen on a fast-OR line (TOUT1-8). A TEM board should ignore these fake fast-OR's while it is loading control register settings.

Table 3. Control Register Contents of Front-end Chip

Bit [a)]	Contents	Remark
0-63	Calibration mask	Bit 0 for channel 0 and bit 63 for channel 63
64-127	Channel mask	Bit 64 for channel 63 and bit 127 for channel 0
128-191	Trigger mask	Bit 128 for channel 0 and bit 191 for channel 63
192-198	Calibration DAC	Bit 192 is the range select (1:high range, 0:low range) Bit 193 is MSB of DAC value and Bit 198 LSB Cal. charge $\approx (0.3 \times (\mathrm{DACvalue} + 1))$ fC in low range Cal. charge $\approx (1.2 \times (\mathrm{DACvalue} + 1))$ fC in high range
199-205	Threshold DAC	Bit 199 is the range select (1:high range, 0:low range) Bit 200 is MSB of DAC value and Bit 205 is LSB Threshold $\approx (6 \times (\mathrm{DACvalue} + 1))$ mV in low range Threshold $\approx (24 \times (\mathrm{DACvalue} + 1))$ mV in high range
206	Readout direction	1:right, 0:left

a) Bit 0 comes first in time.

A control register of a controller chip consists of 7 bits, 1 bit of which is not used and 6 of which are summarized in Table 4. When a control register is loaded with a

specific address or a broadcast address, a controller chip specified with the address outputs previous contents of the register on data output DOUT (differential CMOS signal), with bit 0 first in time. With a broadcast address only contents from the bottom layer will be seen at a TEM board. So far, a TEM board cannot capture nor store this bit stream. So a TEM board should keep track of control register contents of all the controller chip in the tracker.

Table 4. Control Register Contents of Controller Chip

Bit [a)]	Contents	Remark
0	Not used	
1	Readout mode	1:Readout the layer even if it didn't generate a fast-OR signal 0:Don't readout if it didn't
2	FCS[a)] attachment	1:Calculate 11 bit FCS and attach it at the end of data 0:No FCS calculated nor attached
3-7	Number of chips	Number of front-end chips to read from the side Bit 3 is MSB and bit 7 LSB.

a) Bit 0 comes first in time.

5.2 GTFE Command

Here is a complete list of commands for a front-end chip. See Table 5 for actual bit streams. Below are brief explanations on the commands.

Load control register Loads control register of the front-end chip.

Read event Starts the front-end chip shifting data out.

End read-event Stops the front-end chip shifting data out.

Clear event Clear one event in FIFO.

Calibration strobe Injects a test pulse into specified channel(s).

Reset chip Reset command decoders, control registers, and FIFO.

Reset FIFO Reset all the contents of FIFO.

5.3 GTRC Command

Here is a complete list of commands for a controller chip. See Table 5 for actual bit streams. Below are brief explanations on the commands. When a controller chip sends a command to front-end chips, it automatically supplies clock signals for front-end chips of an appropriate number of clock cycles depending on the command.

Load GTRC register Loads control register of the controller chip.

Read event Starts a readout sequence of an event; on receipt of this command, the controller chip sends a read event command to front-end chips with a broadcast address, supplies clocks to front-end chips to shift out data, reads in hit status being sent and store it to an event buffer, and sends an end-read-event command to front-end chips with a broadcast address.

Clear event Clears one event and sends a clear event command to front-end chips with a broadcast address if necessary

Load GTFE register Lets the controller chip send a load control register command to specified front-end chip(s)

Calibration strobe Lets the controller chip send a calibration-strobe command to specified front-end chip(s)

Turn on clock Force the controller chip to turn on clock output for front-end chips. Once a turn-on-clock command is sent to a controller chip, there is no way to stop the clock except for a reset-GTRC command, a reset pulse, and turning off the power.

Reset GTRC Resets control register and readout flags of the controller chips. Also, it stops an action in progress immediately if any.

Reset GTFE Lets the controller chip to send a reset-chip command to specified front-end chip(s).

Reset GTFE FIFO Lets the controller chip to send a reset-FIFO command to specified front-end chip(s).

5.4 Resetting Chips

There are a three ways to reset a front-end chip or a controller chip; by command, by a reset pulse, or by turning on power. The result of resetting varies depending on how it is reset as described below.

Table 5. Commands for a front-end chip GTFE64 and a controller chip GTRC

Chip	Command	Bit sequence (in time order)
GTFE	No-op	1 000 $f_0f_1f_2f_3f_4$
	Load control register	1 100 $f_0f_1f_2f_3f_4$ $d_0d_1\cdots d_{206}$
	Read event	1 010 $f_0f_1f_2f_3f_4$
	Clear event	1 001 $f_0f_1f_2f_3f_4$
	Calibration strobe	1 110 $f_0f_1f_2f_3f_4$
	Reset chip	1 101 $f_0f_1f_2f_3f_4$
	Reset FIFO	1 011 $f_0f_1f_2f_3f_4$
	End read-event	1 111 $f_0f_1f_2f_3f_4$
GTRC	Load GTRC register	1 $a_4a_3a_2a_1a_0$ 000 $r_0r_1r_2r_3r_4r_5r_6r_7$
	Clear event	1 $a_4a_3a_2a_1a_0$ 001
	Read event	1 $a_4a_3a_2a_1a_0$ 010
	Load GTFE register	1 $a_4a_3a_2a_1a_0$ 011 1 100 $f_0f_1f_2f_3f_4$ $d_0d_1\cdots d_{206}$
	Turn on clock	1 $a_4a_3a_2a_1a_0$ 100
	Calibration strobe	1 $a_4a_3a_2a_1a_0$ 101 1 110 $f_0f_1f_2f_3f_4$
	Reset GTFE	1 $a_4a_3a_2a_1a_0$ 110 1 101 $f_0f_1f_2f_3f_4$
	Reset GTFE FIFO	1 $a_4a_3a_2a_1a_0$ 110 1 011 $f_0f_1f_2f_3f_4$
	Reset GTRC	1 $a_4a_3a_2a_1a_0$ 111

a_i : i-th bit of a controller chip address. a_4 is MSB.
f_i : i-th bit of a front-end chip address. f_4 is MSB.
r_i : i-th bit of control register of a controller chip. r_0 is Bit 0 in Table 4.
d_i : i-th bit of control register of a front-end chip. d_0 is Bit 0 in Table 3

A reset pulse is a single-ended CMOS digital signal. There is a reset pad both on a front-end chip and on a controller chip, and they are connected on an HDI together. Also, they are connected to each other on a Kapton readout cable. Therefore, if you send a reset signal to one of the cables, you are resetting all the front-end chips and the controller chips connected on the cable.

Reset pulse A reset pulse resets a command decoder of the front-end chip. It does *not* change contents of control register. A reset pulse to a controller chip resets resets control register and readout flags of the controller chip. So, if you send a reset pulse to the tracker, you have to reconfigure controller chips but not front-end chips.

Reset-chip command to front-end chip A reset-chip command to a front-end chip resets a command decoder, a control register, and FIFO. Note, if you send a reset-chip command to front-end chips, you should reload control register of the front-end chips.

Reset-chip command to controller chip A reset-chip command to a controller chip resets readout flags, but *not* its control register. To maintain consistency between front-end chips and a controller chip, you should reset FIFO's of front-end chips also, when you send a reset-chip command to a controller chip.

Reset-FIFO command to front-end chip A reset-FIFO command resets a FIFO of specified front-end chip(s), namely, erases all the contents of the FIFO.

Power-on Reset Both a front-end chip and a controller chip has a power-on reset feature. It sets a default setting to a control register, clears a FIFO, resets a command decoder, and so on.

5.5 Readout Cable and Repeater Board

There are 8 Kapton readout cables attached to the tracker. Each of cable connects 8 HDI's facing on one side of the tracker to a repeater board attached to the tracker. Signals from the tracker is buffered at a repeater board and sent to a TEM board. Signals from a TEM board is not buffered. Repeater boards are powered by DVDD, or a digital power for an HDI.

A 37-pin Nanonics connector is mounted on the DAQ side of a Kapton cable and connects it to a repeater board. A Kapton cable has 8 "legs", each of which connects an HDI with a 25-pin Nanonics connector mounted on the leg. Pin-assignment of both connectors are in Tables 6 and 7.

5.6 Readout Software

Details about software to readout the tracker is described below.

Table 6. Signals on 37-pin Connector on Kapton Flexible Cable

Pin	Signal	
1	RESET	Reset pulse to HDI
2	AVDD2	2nd analog power supply
3	AGND	Analog ground
4	AVDD	Analog power supply
5	BIAS	Detector bias
6	TEMP1/1	Temperature sensor 1
7	TEMP1/2	
8	TEMP2/1	Temperature sensor 2
9	TEMP2/1	
10	TOUTP8	Fast-OR from 8th layer
11	TOUTN8	
12	TOUTP7	Fast-OR from 7th layer
13	TOUTN7	
14	TOUTP6	Fast-OR from 6th layer
15	TOUTN6	
16	TOUTP5	Fast-OR from 5th layer
17	TOUTN5	
18	TOUTP4	Fast-OR from 4th layer
19	TOUTN4	
20	TOUTP3	Fast-OR from 3rd layer
21	TOUTN3	
22	TOUTP2	Fast-OR from 2nd layer
23	TOUTN2	
24	TOUTP1	Fast-OR from 1st layer
25	TOUTN1	
26	TACKN	Trigger acknowledge to HDI
27	TACKP	
28	CLKN	Clock to HDI
29	CLKP	
30	CMDN	Command to HDI
31	CMDP	
32	DATIN	Data from HDI
33	DATIP	
34	TOKON	Token to HDI
35	TOKOP	
36	DGND	Digital ground
37	DVDD	Digital power supply

Table 7. Signals on 25-pin Connector on i-th leg of Kapton Flexible Cable

Pin	Signal	
1	RESET	Reset pulse to HDI
2	AVDD2	2nd analog power supply
3	AGND	Analog ground
4	AVDD	Analog power supply
5	BIAS	Detector bias
6	TEMPn/1	Temperature sensor n (if assigned[a)])
7	TEMPn/2	
8	TOUTPi	Fast-OR to TEM
9	TOUTNi	
10	TACKN	Trigger acknowledge from TEM (bus)
11	TACKP	
12	CLKN	Clock from TEM (bus)
13	CLKP	
14	CMDN	Command from TEM (bus)
15	CMDP	
16	DATIN	Data to the lower layer (daisy-chained)
17	DATIP	
18	DATIN	Data from the higher layer (daisy-chained)
19	DATIP	
20	TOKON	Token to the higher layer (daisy-chained)
21	TOKOP	
22	TOKON	Token from the lower layer (daisy-chained)
23	TOKOP	
24	DGND	Digital ground
25	DVDD	Digital power supply

a) A temperature sensor line is connected only on two legs of a Kapton cable. The location of the legs varies.